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Kwame Osei Boateng

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STAAS & HALSEY LLP

SUITE 700

1201 NEW YORK AVENUE, N.W.

WASHINGTON, DC 20005

EXAMINER

SIEK, VUTHE

ART UNIT

PAPER NUMBER

2825

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Please find below and/or attached an Office communication concerning this application or proceeding.



### **DETAILED ACTION**

1. This office action is in response to application 09/985,768 and response filed on 9/1/2006. Claims 1-14 remain pending in the application.

#### ***Claim Rejections - 35 USC § 101***

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 14 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The above claimed invention appears to be to an abstract idea than a practical application of the idea. The claimed invention does not result in an output transformation that provides a useful, concrete and tangible result. Note that a tangible requirement does require that the claim must recite more than a 101 judicial exception, in that the process claim must set forth a practical application of that 101 judicial exception to produce a real-world result. Therefore, the claimed invention appears non-statutory.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Pomeranz et al., "On Static Compaction of Test Sequences for Synchronous Sequential Circuits," ACM, 1996, pages 1-6.

7. As to claims 1 and 10-13, Pomeranz et al. teach substantial same method/apparatus/a computer readable medium storing a program for performing compaction of a set of test stimuli (test sequences) for a digital circuit (see pages 1-6) comprising performing a simulation on a digital circuit with a set of test stimuli to trace faults which the set of test stimuli cover (performing fault simulating); selecting essential test stimuli (vector selection) from among subsets of the set of test stimuli after mapping between the test stimuli and the faults has been established by the simulation, an essential test stimuli being a test stimulus that detects at least one fault, which is detectable by no other test stimulus in one of the subsets of test stimuli; eliminating redundant test stimuli from among subsets of the test stimuli after selection of the essential test stimuli from each subset, a redundant test stimulus being a test stimulus that detects a fault, which is detectable by another test stimulus in each subset after the selection of the essential test stimuli (compaction based on vector selection); and outputting a compacted set (see section 5, pages 4-5). Note that the process for compacting test sequences (test stimuli) based on vector selection as taught by Pomeranz et al. is executable by a computer program stored on a computer readable medium on a computer. The method as taught by Pomeranz et al. provides several advantages: the compacted sequences (compacted test stimuli) have shorter test application time and smaller memory requirement (see concluding remarks on page 6).

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In addition, the compaction based vector selection of a minimal subset of subsequences sufficient to detect all the faults detected by the original sequence (see page 1).

8. As to claim 14, the claim limitations of selecting essential test stimuli (test patterns); and eliminating redundant test stimuli after selection of the essential test stimuli are taught by Pomeranz et al. (see section 5 pages 4-5).

9. As to claim 2, Pomeranz et al. teach outputting a reduced set of test patterns (a compaction procedure based on selection of a minimal subset of subsequences is sufficient to detect all the faults detected by the original sequence) (see page 1, section 5 pages 4-5), which covers faults detectable by the set of test stimuli without modifying test stimuli in the minimum-sized subset, as the compacted set.

10. As to claim 3, Pomeranz et al. teach hierarchically repeating the selection of essential test stimuli (compaction based on vector selection) from among subsets of remaining test stimuli after elimination of redundant rest stimuli from the subsets, and outputting the compacted set comprising the selected essential test stimuli (see section 5 pages 4-5).

11. As to claim 4, Pomeranz et al. teach the elimination includes identifying a subset of test stimuli that optimally covers a given set of faults and eliminating one or more test stimuli other than the identified test stimuli as the redundant test stimuli (a compaction procedure based on selection of a minimal subset of subsequences is sufficient to detect all the faults detected by the original sequence (see page 1, section 5 pages 4-5)).

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12. As to claim 5, Pomeranz et al. teach storing information of the set of test stimuli, information of faults, which the set of test stimuli cover in matrix form. Pointing information associating each test stimuli with the faults detectable by corresponding test stimuli must be also be stored, so that such information must be used by process of selecting and eliminating (see section 5, pages 4-5). Using pointers is a common practice in the art, therefore the compaction procedure based on selection of a minimal subset of subsequences that is sufficient to detect all the faults detected by the original sequence must use pointer during mapping process.

13. As to claim 6, Pomeranz et al. teach the claim limitations in section 5 (see pages 4-5). Note that Pomeranz et al. teach fault simulating the sequence and collecting all the subsequences that detect every fault and use a coverage procedure to select a minimal subset of subsequences to detect all faults. The counter must be used during to process in order collect test sequences and every faults detected.

14. As to claim 7, Pomeranz et al. teach stuck fault test pattern generation (see section 5, pages 4-5).

15. As to claim 8, Pomeranz et al. teach compaction based on vector selection, where the compaction procedure based on selection of a minimal subset of subsequences that is sufficient to detect all the faults detected by the original sequence (see page 1, section 5 pages 4-5). Since delay fault is a common practice when testing a digital circuit, the compaction based on vector selection must also detect faults of a delay fault model.

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16. As to claim 9, Pomeranz et al. teach performing compaction of the set of test stimuli by regarding a sequence of initializing, sensitizing and propagation subsequences as a single test stimulus (at least see section 5, pages 4-5).

**Remarks**

17. Examiner has reviewed the arguments that appear to be persuasive. Since, the claimed invention is not novel, Examiner submits new grounds of rejection. Pomeranz et al. teach all claim limitations (see pages 1-6, specifically pages 4-5).

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Vuthe Siek

  
VUTHE SIEK  
PRIMARY EXAMINER